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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/693,568	10/24/2003	Patrick Lysaght	X-1374 US	1995

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EXAMINER	
LEVIN, NAUM B	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 06/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/693,568	LYSAGHT ET AL.	
	Examiner	Art Unit	
	Naum B. Levin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *01/03/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/693,568, and Amendment filed on 03/31/2006. Claims 1,11, 14 and 17 have been amended by including additional limitation. Claims 1-20 remain pending in the application.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-8 and 10-20 are rejected under 35 U.S.C. 102(e) as being unpatentable by Chen (US Patent 6,687,888).

3. As to claims 1, 11, 14 and 17 Chen discloses:

(1), (11), (14) A method/program/computer of designing an integrated circuit having a plurality of logic paths, comprising (col.13, ll.20-25, col.13, ll.37-40):

designing the integrated circuit in accordance with timing constraint data (constraint file/delay limits/timing constraints) (col.3, ll.49-67);

identifying any logic paths (circuit paths/paths) in said plurality of logic paths that have a timing characteristic within a threshold (Delay for each path from clock to clock in the partition is calculated, and each delay total is compared to timing constraints-col.8, ll.50-52) to define a first set of logic paths (This includes devices that may not be

related to critical paths-col.12, ll.49-50-non-critical paths; path B 704 ... need not, also be a critical path-col.12, ll.28-30), where any logic paths in said plurality of logic paths other than said first set of logic paths define a second set of logic paths (If any path exceeds timing constraints, the score for the individual is negatively affected-col.8, ll.52-54-critical paths) (col.8, ll.49-57; col.9, ll.53-58; col.12, ll.28-30 Fig.7); and

selectively optimizing the integrated circuit to reduce power consumption in response to said first set of logic paths and said second set of logic paths (It has been found advantageous during partitioning 402, 604 to include all branches of a critical path in the same partition, that is then subjected to optimization on all elements of the partition-col.12, ll.34-37; All devices, other than those flagged with a "do not touch" flag and those that are part of clock trees balanced by a separate optimizer, are included in optimization. This includes devices that may not be related to critical paths. Optimizing devices unrelated to critical paths allows the optimizer to reduce overall power consumption by resizing and changing device types of these devices- col.12, ll.46-53) (col.12, ll.20-53; Fig.7);

(17) A method of designing an integrated circuit, comprising:

designing the integrated circuit in accordance with timing constraint data (col.3, ll.49-67);

identifying timing critical logic circuitry (col.8, ll.49-57; col.9, ll.53-58; col.12, ll.28-30 Fig.7); and

selectively optimizing the integrated circuit to reduce power consumption in response to said timing critical circuitry (col.12, ll.20-53; Fig.7).

4. As to claims 2-8, 10, 12-13, 15-16 and 18-20 Dean recites:

(2), (12), (15), (18) The method/program/machine, wherein said selectively optimizing comprises power optimizing only said second set of logic paths (col.12, ll.20-45);

(3), (5) A method, wherein power optimizing comprises placing first and second set of logic with respect to target device, and routing connections of said first an second set of logic paths (col.7, ll.19-57; col.6, ll.24-43);

(4), (7), (13), (16), (19) The method/program/machine, wherein said selectively optimizing comprises power optimizing said first set of logic paths and said second set of logic paths, and determining whether said timing characteristic of any logic paths in said first set of logic paths has been modified beyond a threshold to define a third set of logic paths ((col.12, ll.8-53; Fig.7));

(6), (8) The method comprises rejecting a power optimization for each logic path in the third set of logic paths (col.4, ll.29-51; col.11, ll.28-42);

(10), (20) The method, wherein said threshold is defined by an absolute value (col.8, ll.49-57).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen in view of Dave (US Patent 6,178,542).

With respect to claim 9 Chen teaches the features above but lacks the method of designing the integrated circuit having the plurality of logic paths, wherein the threshold is defined by a percentage of parameter in the timing constraint data.

As to claim 9 Dave in view of Chen teaches:

the method, wherein the threshold is defined by a percentage of parameter in the timing constraint data (A very high utilization of programmable functional units and pins may force the router to route the nets in such a way that it may violate the delay constraint, i.e. the worst-case execution times defined by the execution time vector ... may be exceeded. In order to address this aspect, the algorithm uses only 70% of the available PFUs and 80% of the available pins for mapping tasks/edges to FPGAs and PLDs during synthesis. These percentages were derived based on existing designs and experimentally verified to guarantee the meeting of delay constraints during co-synthesis) (Abstract; col.5, ll.25-46).

It would have been obvious to a person of ordinary skills in the art at the time the invention was made to employ Dave's teaching regarding the method of designing the integrated circuit having the plurality of logic paths, wherein the threshold is defined by a percentage of parameter in the timing constraint data and use it in Chen's invention to guarantee the meeting of delay constraints during the design of programmable logic devices, thereby specifically increasing an efficiency of the programmable logic devices design.

Remarks

6. Mostly Applicant argues: "Chen does not teach or suggest "designing the integrated circuit in accordance with timing constraint data to produce a design result"".

Chen, for example, recites: "Much design of complex integrated circuits is accomplished through a design flow (col.3, ll.49-50)... Static timing analysis software is then used to determine expected delays in a circuit, and to compare these delays with limits expressed in a "constraint file. (col.3, ll.57-60)" ... Results of this preliminary timing analysis are often fed back to the synthesis tool, which substitutes faster gates, and may rearrange logic, as necessary to meet timing requirements (col.3, ll.64-67)".

7. Next, Applicant argues: Chen does not teach or suggest ..." selectively optimizing the integrated circuit to reduce power consumption ...".

Chen, e.g., describes: "It has been found advantageous during partitioning 402, 604 to include all branches of a critical path in the same partition, that is then subjected to optimization on all elements of the partition (col.12, ll.34-37)"

Chen, e.g., also teaches: "All devices, other than those flagged with a "do not touch" flag and those that are part of clock trees balanced by a separate optimizer, are included in optimization. This includes devices that may not be related to critical paths. Optimizing devices unrelated to critical paths allows the optimizer to reduce overall power consumption by resizing and changing device types of these devices (col.12, ll.46-53)".

8. Applicant also argues: "The design result is a complete result optimized for timing only. ... Thus, in Applicants' claim 1, an integrated circuit is first designed in

conformity with timing constraint data to produce a design result (e.g., a timing-driven process) and then optimized to reduce power consumption (e.g., a power-driven process)."

Examiner appreciates the detailed remarks offered by Applicants, however claim 1 not recites these specific particular limitations.

9. As to claim 9, Applicant argues that because Chen does not teach all limitations of claim 1 the combination of Chen and Dave does not satisfy the requirements of 35 U.S.C. 103(a) rejection.

As shown above Chen teaches or suggests all limitations of independent claim 1, thereby rejection of claim 9 fully satisfies the requirements of 35 U.S.C. 103(a) rejection.

10. Examiner defined Applicant's arguments as none persuasive.

Accordingly **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B. Levin whose telephone number is 571-272-1898. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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VUTHE SIEK
PRIMARY EXAMINER